

Dhaval J. Brahmbhatt
Intellectual Property Consultant Curriculum Vitae

Dhaval J. Brahmbhatt

Areas of Expertise

- Patent review
- Patent analysis
- IP Negotiations
- Language Interpretation
- Technology Commercialization
- International Collaborations

Professional Summary

Mr. Brahmbhatt brings over 30 years of experience in high-tech industry as an Engineer, Technologist, and as a Senior Executive. He is a serial entrepreneur listed on the prestigious Silicon Valley Genealogy Tree for the 1983 EPROM, EEPROM and non-volatile programmable logic technology based startup, ICT Inc. (which went public in 1989). He is a creative engineer with 11 US patents awarded - 10 as the sole inventor, and as the lead inventor in all eleven - many in the area of memory IC design, Analog IC design and device physics. Mr. Brahmbhatt brings litigation experience as expert witness of over 18 years and have been involved specifically in the cases that involve Flash memory modules, DRAMs, SRAMs, firmware, sub-systems, IC, device physics, etc. Mr. Brahmbhatt has been deposed many times as expert witness and brings experience at ITC, U.S. District Courts, State Courts, etc. In addition to being an expert for the plaintiff and defense, he also brings the experience of working as technical expert for a US District judge.

Mr. Brahmbhatt started his career at Fairchild Semiconductor in 1978 following graduate school and started working in the design and product development of MOS memory and micro-processor with onboard NVM. He then worked on single power supply semiconductor non-volatile EEPROM memory chips at Synertek (a subsidiary of Honeywell) and later at National Semiconductor where he worked on EPROM compatible high density EEPROM memory chips. Following this, he founded with four colleagues, International CMOS Technology (ICT) in 1983 that was focused on programmable memory and programmable logic IC products. Following the initial public offering (IPO) of ICT, Mr. Brahmbhatt then re-joined National Semiconductor as Product Line Director where he was in charge of EPROM business Product Line and supervised close to 100 highly qualified professionals. He had complete responsibility for design, product engineering, testing, customer relations and P & L of a \$150 million business unit. Mr. Brahmbhatt worked at National Semiconductor until 1996.

After National Semiconductor, Mr. Brahmbhatt was Vice-President of a major SIMM/DIMM DRAM and Flash EEPROM memory module manufacturer, Smart Modular. Here Mr. Brahmbhatt designed Flash PCMCIA and CompactFlash memory modules and participated in industry standardization committees for CompactFlash. After Smart Modular, Mr. Brahmbhatt then consulted in Flash memory card industry. Following this, he was involved as "C" level

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executive with couple startups (one got acquired) before starting his current company, PHYchip Corporation that is now over ten years old. At PHYchip Corporation, Mr. Brahmbhatt has taken a variety of IP Expert Witness assignments, in Flash and other memory IC including DRAMs and SDRAM memory and also memory modules/sub-systems.

Mr. Brahmbhatt is a registered Language Interpreter for 5 south Asian languages (from India) and one language from Fiji. He is listed with the Judicial Council of California to work with State and Federal courts. He is the past elected Board Member of California Healthcare Interpreters Association (CHIA, Board Member until 12/31/13).

Has over five years of experience of reviewing SBIR/STTR grant applications for various agencies of the United States Government in subjects ranging from Advanced Semiconductors, Software, Hardware, Nanotechnology, MEMS/NEMS, Sensors, Wireless/Optical/Wired Communications, etc.

Mr. Brahmbhatt has taught at Santa Clara University Graduate School of Engineering and Ohlone College as Adjunct Faculty. He also taught courses at SPIE annual conferences in Nanotechnology and Alternate Energy fields. Mr. Brahmbhatt is an active member of the IEEE (IEEE Senior Member), and is the Founder and now Chairman Emeritus of the IEEE SF Bay Area Nanotechnology Council. He has been recognized numerous times by the IEEE with citations and awards, and is the recipient of the IEEE 2008 CY Award for Outstanding Leadership and Professional Services. Mr. Brahmbhatt is the past President of the prestigious Silicon Valley Engineering Council. He is currently the Chair of the IEEE Vehicle Technology Society of San Francisco Bay Area.

Patents with Mr. Brahmbhatt as the sole inventor on 10 out of 11 patents, and as the lead inventor on all patents listed below

<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
5,646,886	1997	Flash Memory Having Segmented Array for Improved Operation
5,583,808	1996	EPROM Array Segmented for High Performance and Method for Controlling Same
5,457,652	1995	Low Voltage EEPROM
5,341,342	1994	Flash Memory Cell Structure
5,016,217	1991	Logic Cell Array Using CMOS EPROM Cells Having Reduced Chip Surface Area
4,910,471	1990	CMOS Ring Oscillator Having Frequency Independent of Supply Voltage (this is the only patent involving a second inventor besides Mr. Brahmbhatt)
4,885,719	1989	Improved Logic Cell Array Using CMOS EEPROM Cells
4,831,589	1989	EEPROM Programming Switch Operable at Low VCC
4,823,317	1989	EEPROM Programming Switch
4,460,979	1984	Memory Cell

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4,442,481 1984 Low Power Decoder Circuit

Education

<u>Year</u>	<u>College/University</u>	<u>Degree</u>
1978	University of Cincinnati, OH	MS, Electrical Engineering
1977	Gujarat University, India	MSc Physics, specialization in Solid State Electronics
1995	Marketing Excellence, University of London, Ontario (Canada)	Certificate
1994	Marketing Management, Stanford University	Certificate
1993	Small Company Management, Stanford University	Certificate
2007	Certified trained Nanotechnologist by California Institute of Nanotechnology	Certificate
2010	Certified Green Building Professional by Build it Green	Certificate
2010	Language Interpreter Registered with California Judicial Council	Certificate & Registered
2011	Energy Efficiency Professional (CA Workforce Devl. & San Jose City College)	Certificate
2011	Notary Public, California	Certificate & Registered
2014	State of California Real Estate Broker	State Certified/licensed

Professional Associations and Achievements

- Founder, Chairman Emeritus, IEEE SF Bay Area Nanotechnology Council
 - Senior Member IEEE
 - Chairman, IEEE Vehicle Technology Society For San Francisco Bay Area
 - Commissioner & Past Chair, Economic Development Commission, City of Milpitas
 - Appointed by Hon. US Congressman Mike Honda on “Blue Ribbon Task Force on Nanotechnology” for the State of California (2005-2006)
 - Past President, Silicon Valley Engineering Council (SVEC)
 - Previous Counselor, Small Business Development Council in San Jose (under SBA)
 - Member of Consultant Network Silicon Valley (CNSV)
 - Listed on Judicial Council of California as registered language interpreter
 - Former Elected Board Member of California Healthcare Interpreter’s Association
 - California Notary
 - California Real Estate Broker License
 - Rotary International Fellowship Award
 - Government of India National Scholarship Award
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