

Harry Peterson

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Highly experienced, Caltech educated chip designer. Former Director of Design Engineering for Toshiba and Fellow of Video Technology for Pixelworks.

Current practice mainly involves:

- **Design and manufacture of high performance data converter circuits**
- **Optoelectronic devices, circuits, packages and systems**
- **RF Integrated circuits and wireless, wired and fiber-optic communications**
- **Development of display chips and systems for medical and consumer systems**
- **Telecommunications reliability, security, efficiency and analytics**
- **IP protection (strategy, patent portfolio acquisition, sale and defense)**
- **Litigation Support/Expert witness**

Summary of Experience

2009-Present Consultant, Yanntek Inc, Silicon Valley, CA

Primary activity: Design

- Use behavioral simulation (e. g. Matlab) to map back-of-envelope concept sketches to rigorous design specifications that can efficiently guide system and circuit implementation.
- Design, simulate and verify devices, circuits, packages and systems.
- Support verification, manufacturability analysis, layout, new-product-bring-up and market-ramp activity.

Here are some of the circuits and systems I have recently designed:

- (1) 14b Sigma-delta ($\Sigma\Delta$) ADC and 12b DAC for highly integrated wideband (terabit per second) fiber optic communications system. Process: B55 (ST SiGe 55nm BiCMOS)
- (2) Extreme-low-jitter clock distribution system for network chip
Developed custom CML blocks for a single-chip network switch that features dozens of PCIe gen3 IO's with extremely tight timing requirement. Process: TSMC 28HPC
- (3) Timing and calibration circuits for a 5Gbps 12b analog-to-digital converter (interleaved SAR), with extreme-low-jitter clock distribution system and calibration circuitry. Process: Global Foundries 65nm

Secondary activity: Advise

Provide support expertise as follows:

- Train design teams in the art of high performance mixed-signal chip simulation and verification
- Drive system-level hardware/software/application integration
- Support of outsourcing and design reviews
- Model-driven analytics and security
- Due-diligence in support of merger and acquisition (M&A) and investment activity
- Expert witness testimony

2009-2013 Board Proxy, Evatronix SA - Warsaw, Poland

Evatronix was an IC design startup launched shortly after Poland regained independence in 1989. My role was to define and implement a high-growth strategy and to achieve a very successful exit. I helped recruit and build two teams of analog designers (Warsaw and Gliwice), supervised and worked alongside them during the first four projects, delivered IP blocks to customers and assisted with bring-up of production chips. Helped negotiate corporate exit (Cadence acquired Evatronix in 2013).

2005-2009 Fellow and Senior Director of Engineering, Pixelworks (Nasdaq: PXLW) - San Jose, CA

Developed hardware and firmware systems used in consumer video products. Optimized performance for 3D and super-resolution applications. Introduced innovative low-cost packages. Built and ramped video-chip design and support teams in Shanghai, San Jose, Portland and Toronto. Led design of complex video chip (PEARL) and helped achieve market wins at Sony, Epson and other companies. Managed NPI (new-product-introduction) activities with foundries and package vendors. Participated in standards development groups (USB3 and VESA). Helped map and execute corporate video-standards strategy (H.264, H.265, DisplayPort).

My principle role during this period was to build a world-class design team in Shanghai, manage an existing portfolio and supervise porting to new processes and applications. We developed data converters, video processing subsystems, and highly integrated, cost-effective SOCs. I also recruited and supervised external contractors who supported our design and development activity.

2003-2005 Director of Design Engineering, Toshiba - San Jose, CA

Managed design and NPI (New Product Introduction) of a family of multi-standard >6Gbps SERDES phy's developed jointly with Rambus. Led the Toshiba North America FAE team for chips and packages. Supervised internal and external design activity for USB, XAUI, Fiber-channel, DDR, PCIe and SATA IP.

Managed definition, acquisition, development and qualification of new IP blocks, and integration in chips.

1989-2003 Consultant, San Jose, CA

Designed 23 chips: RFIC (LNA, mixer, VCXO, ADC, DAC, integrated-baseband, et cetera), ultra-low-power data-converters and communication links, and other analog and digital applications. Much of my work involved CMOS and MEMs sensors required in ultra-precise imaging, navigation and communication systems. Typical use-case scenarios involved military, space, medical and commercial applications.

During this period I designed many data converters, precision timing and power-management circuits. Technologies included NMOS, CMOS, buried-channel CCD, bipolar and biCMOS. Data converters I designed during this period used the following circuit topologies: Sigma-delta, pipeline, flash, SAR.

Served as business advisor to semiconductor companies contemplating mergers and acquisitions.

Served as expert witness on several patent-infringement cases involving analog circuit technology.

1988-1989 Analog Wizard, Echelon (Nasdaq: ELON) - Los Gatos, CA

Designed chips that implemented IOT-like system of sensors, RF and PLC communication links and embedded processors for home and building automation. ELON, where I was employee number 7, is now part of Adesto (NASDAQ: IOTS).

1980-1988 Consultant, Lac Supérieur, QC, Canada

Designed many analog signal-processing and data-converter chips for my customers, including LeCroy (now Teledyne), Fairchild, National Semi, Intersil, Hewlett-Packard, Westinghouse, and Teradyne. Provided supply-chain support.

1978-1980 Senior Manager, IC Development, Bell-Northern Research (Nortel Networks) Ottawa, Canada

Nortel Networks, a very large Canadian telecommunications company, hired me to achieve technical turnaround of a critical chip-design project, which had suffered a series of painful failed tapeouts. I redesigned 14-bit ADC, DAC and filter circuits, supervised fabrication in external and internal foundries, and managed chip bring-up and qualification activity. This SOC (QMV59) was the first successful MOS filter-codec ASIC, and it was the key enabler of the DMS100 telecom switch. NT's DMS business quickly grew to about half a billion dollars per year. I launched the successor to this chip (E47), which moved key elements of the design from buried-channel CCD technology to switched-cap cmos, which allowed further cost reduction and scaling. I was promoted to manager of all IC-design and package-development activity within Northern Telecom.

1977-1978 Manager, Custom IC Design Group, Philips Corporation (Signetics) - Sunnyvale, CA.

My team designed Sigma-delta ADC's, digital processors, RF synthesizers, and avionics subsystems. Provided support for external foundry customers. Managed contractors and design-service vendors.

1975-1977 Manager, CAD Group, Eastman Kodak Corporation - Rochester, NY

Designed mixed-signal chips for miniaturization and cost-reduction of video cameras. Supervised team of layout and CAD engineers who did physical design and verification of imaging chips.

1974-1977 Experimental physicist, Stockholm Observatory - Saltsjöbaden, Boulder and La Palma

Member of the joint Swedish/NASA team that ran solar-physics experiments on OSO-8 (Satellite).

Designed and built instrumentation for Observatorio del Roque de los Muchachos (administered by Stockholm Observatory, in the Canary Islands). Devised a novel Fabry-Perot spectroscopy technology and a single-photon-counting imaging system which achieved unprecedented sensitivity.

1973-1975 Device Physicist, Fairchild Semiconductor - Palo Alto, CA

Ran process simulations and semiconductor fab equipment to develop and prototype a super-fast bipolar process called I3L. Provided modeling and device support for chip design and qualification teams who used I3L to design and manufacture the 93481 family of fast DRAM chips.

Publications since 2010

"Design Principles and Realization of Electro-Optical Circuit Boards," SPIE Photonics West, 2013

"Communicating Basic Process Parameters and Criteria for Mixed-Signal and RF Processes," article in GSA FORUM, March 2011

"Systematic approach to verification of a mixed signal IP - HSIC PHY case study," IEEE IP SOC 2010, Grenoble

Presentations

"Behavioral Modeling facilitates Chip-Package Co-design," Cadence user conference (CDNLive!), 3 May 2011, Munich

"Low cost high-performance packages," invited talk at Warsaw University of Technology Conference, April 2009, Warsaw

"EDA implications of advances in video chips," presented at Mentor Graphics Workshop, February 2007, Wilsonville

"Integrating Physical Test into the IC Studio Workflow", U2U CAD Conference, February 2007, Santa Clara

"Where submicron CMOS Meets Acoustic Holography," Caltech Conference, February 2005, Palo Alto

"A Flex architecture for systems with embedded, spatially-distributed sensors," Flexible Electronics Workshop, Max Planck Institute, June 2003, Leipzig

"Sandstorm: Embedded Electronics for Spatially Diverse Sensors," IEEE Signal Processing Society SCV, December 2003, Sunnyvale

"The Quest for Greater-than-100dB on-chip Isolation," IEEE Workshop, April 2002, San Jose

Education

California Institute of Technology, Pasadena, CA. BS '70 Physics

NASA (Goddard)

Stockholm Observatory, Saltsjöbaden, Sweden.

U.S. Patents Granted or Pending

#4021786 Memory cell circuit and semiconductor structure therefore

#20110242305 Immersive Multimedia Terminal

#2018157122 High Speed Wireless Data Network

#20180175180 Millimeter wave communication system

#20180248612 Millimeter wave communications through obstructions

#20180302238 High-speed wireless multi-path data network

Expert Witness/Litigation Support Experience

Testifying, writing expert witness reports, and presenting at *Markman* hearings