SIAMAK ARYA

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ARCHITECT AND CONSULTANT

Processor, Chip Set, Controller, and System Design...Performance Engineering

An accomplished executive and architect with over 30 years of experience in processor, chip set, controller, and system design and performance engineering for computational, consumer, DSP, and Media applications. Over 23 years of management experience.

PROFESSIONAL EXPERIENCE

GREENLIANT SYSTEMS, Santa Clara, CA **5/2010 - Present**

Chief Technology Officer
Responsible for technology, innovation, and design of future storage products including controllers, cards, and drives.

Responsible for design and development of Greenliant's first generation high capacity and performance Enterprise SSD.

Responsible for design of Greenliant's second generation very high capacity and performance Enterprise SSD.

SILICON STORAGE TECHNOLGY, Sunnyvale, CA **6/2007 – 5/2010**

Sr. Director, Systems Architecture
Responsible for the system architecture of all NAND controllers.

- Defined and enforced a system design process from feature definition through implementation.
- Designed 4 sophisticates SSD controller architectures.
- Modified and improved the architecture of a high capacity SIM card.
- Designing the next generation SSD controller architecture. Represented SST at international standards committees such as JEDEC and ETSI.
- Leading an advanced development group in exploring new innovations.

SYMANTEC CORPORATION, Mountain View, CA **9/2005 – 1/2007**

Director, Performance Engineering
Responsible for performance analysis, improvement, and scalability of Symantec's storage products. Managing teams in Mountain View and India.

- Elevated the group from performance testing to performance engineering at early development phase
- Evangelized and Engaged the group in competitive analysis for goal setting and marketing data
- Set up a process and procedure for project engagement, prioritization, and planning
- Initiated 17 product improvement projects with many significant results

SIAMAK ARYA CONSULTING, Cupertino, CA **4/2004 - present**

President/ Principal Architect
Consulting in system and processor design and development, performance analysis and projection, and system and application optimization. Consulting and design projects included:

- Extensive patent infringement consulting in processor architecture and design
- Architecture and micro-architecture design for an HD H.264 & VC1 decoder including motion compensation and deblocking units, data format definition, memory impact analysis, and synchronization & interfaces.
- VOIP and voice recognition
- Networking
- Cache design and algorithm analysis

TELAIRITY SEMCONDUCTOR, INC., Santa Clara, CA **1/2002 – 3/2004**

Vice President, System Engineering 5/2002 – 3/2004
Responsible for architectural design, instruction set and performance simulator, C/C++ vectorizing compiler, performance, application and algorithm analysis, vector libraries, and test code. Additionally, I had sales and marketing responsibilities.

- Co-architected a new Multi-pipe vector-Media / DSP processor for high speed video solutions.
- Designed the Vector-Media instruction set for the vector processor.
- Led and managed performance, application, and algorithm analysis
- Specified performance simulator and C/C++ vectorizing compiler, and drove their implementation
- Architected 3 DSP architectures (4 wide SIMD FFT and FIR, and a single FIR)
- Defined a complete set of blocks for Telairity's digital design technology.
- Performed duties of sales, sales support, marketing, and customer relationship. And, managed operations for a short time.

Director, Architecture **1/2002 – 4/2002**

Led and managed the design of DSP architectures and complete block definition for Telairity's block based design technology.

ARC CORES, INC., San Jose, CA **9/2000 – 10/2001**

Director, Architecture
Led and managed the design and development of Arc's next generation high performance, low power, and configurable embedded-processor, with special features for DSP and Media applications.

- Managed and led architects, micro-architects, compiler engineers, simulation engineers, and performance engineers to design a new ISA and microarchitecture.
- Participated in all phases of the design. The design was a statically scheduled, in-order-issue, SIMD, VLIW, and configurable processor.

APPLE COMPUTER, INC., Cupertino, CA **2/1998 – 9/2000**

Director, Architecture and Performance
Responsible for architectural and performance analysis of Apple's systems and chips.

- Worked with the chipset designers to define and evaluate future chipsets.
- Managed the investigation and resolution of performance issues on existing systems in order to produce higher performance systems. Major issues were resolved on memory controller, graphics, ethernet, etc.

- Managed the system performance evaluation and projection activities including processor, memory, IO, and graphics. Drove the resolution of all issues to satisfaction.
- Led the development of workloads and performance metrics for application based performance evaluation.
- Worked with marketing and product groups to generate performance projections for the new system architectures to satisfy marketing requirements.
- Interfaced with Motorola on the design of PowerPC processors for Apple.
- Managed the development of a simulation platform for architectural evaluation from concept to detailed design.
- Managed up to 22 architects, performance engineers, and modeling engineers.

SILICON GRAPHICS, INC., Mountain View, CA **6/1995 – 1/1998**

Manager, Architecture and Performance
Responsible for desktop system architecture and performance.

- Developed a system level simulation and application analysis platform for the design of new systems and performance analysis.
- Drove the design of a new multiprocessor memory controller and optimization of the existing one.
- Interacted with engineering groups, including the OS and application groups, and determined system requirements and its impact on the system architecture.
- Developed workloads and used standard benchmarks, graphics and SPEC, for performance evaluation and system design.

SUN MICROSYSTEMS, INC., Sunnyvale, CA **11/1991 – 5/1995**

Senior Staff Engineer 1/1994 – 5/1995
Responsible for the design of a new VLIW processor.

- Continued the design of the Intergraph VLIW processor.
- Evaluated and interacted with Sun's Russian team on the design of their VLIW processor

INTERGRAPH CORPORATION, APD, Palo Alto, CA, (acquired by Sun) **11/1990 – 12/1993**

Director, Architecture and Performance
Responsible for the next generation, very-high performance and parallel issue (VLIW) processor architecture. Responsible for performance analysis of Intergraph's Clipper processors.

- Co-architected a new VLIW processor and designed its instruction set for Intergraph..
- Managed the development of a compiler for the new processor.
- Led and managed evaluation of Intergraph's processors and issued the official performance numbers for publication.
- Represented Intergraph at SPEC, before and after Intergraph's election to the SPEC Steering Committee.
- Managed up to 24 architects and performance engineers, simulation engineers, and compiler engineers.
- My VLIW patents US05560028 and US06360313 have so far gained Intergraph Corporation $268M from Intel and Texas Instruments.

UNISYS CORPORATION **11/1990 – 11/1991**

Manager, Architecture and Modeling
Responsible for overall system architecture design issues, system performance evaluation and modeling, performance measurement, and fault tolerant design.

- Organized the architecture team, identified design issues, and resolved them.

- Brought hypercube interconnection project in-house, from Jet Propulsion Labs, and completed the design.
- Managed and led the development of simulation models, instrumented a processor to collect traces of TPC-C, and resolved architecture and performance issues.

AMDAHL CORPORATION 10/1989 – 11/1990

Principal Computer Architect
Responsible for the evaluation of Amdahl's scientific supercomputer.

- Evaluated, analytically and through simulation, the performance of the new architecture and recommended performance enhancements to memory and IO subsystems. All recommendations were implemented.
- Participated in the selection of the processor for the next generation system.

GOULD ELECTRONICS 7/1983 – 8/1989

Principal Member of Technical Staff II (Sr. Sect. Mgr.) 1/1989 – 8/1989
In addition to the responsibilities as Section Manager, responsible for the development of optimized vector libraries for Gould's mini supercomputer products.

- Lead a team of 3 people in developing BLAS1, 2, and 3, Linpack, and FFT libraries to achieve a 2-5 times speed up over Fortran.

Principal Member of Technical Staff I (Sect. Mgr.) 1/1987 – 1/1989
Responsible for parallel processing project for Gould's NPL product line; architectural design of a parallel processor system, including a vector supercomputer, for Gould's mini supercomputers.

- Designed the hardware and software architectures for parallel processing project. The project involved 3 geographically distant sites. Managed a team of up to 8 senior engineers in a matrix organization.
- Principal architect of a design team to design Gould's future vector processor (FP1). Designed the instruction set and the architecture for a 64-bit vector supercomputer.

Senior Scientist 1/1986 – 12/1986
Responsible for supercomputer design project for government.

- Proposed and secured government and company funding for the architectural design of a highly parallel supercomputer (Tera Flop system)
- Designed and proposed the development of such a system including the hardware, software, and operating system. Project also involved coordination of 6 senior staff members in 4 geographically distant sites, and making numerous presentations to the customer and the top management.

Scientist 7/1983 – 1/1986
Responsible to support Gould's divisions in advanced architecture research.

- Evaluated Gould's new mini-vector-computer and proposed changes improvement that were implemented.
- Designed a Gallium Arsenide RISC microprocessor.
- Participated in the design of various systems across multiple divisions (Computer Systems and Defense).
- Proposed an architectural simulator.
- Implemented a TCP/IP software package with another colleague.

Available Upon Request **2/1974 – 6/1983**

EDUCATION:

- Ph.D., Computer Engineering, the University of Michigan, Ann Arbor, Michigan, 1983.
- M.S.E, Computer Engineering, the University of Michigan, Ann Arbor, Michigan, 1979.
- B.S.E., Electrical Engineering, Arya Mehr University of Technology, Tehran, Iran, 1974.

PROFESSIONAL CONTRIBUTIONS

ISSUED PATENTS:

US07724568	02/29/2008	Memory device having read cache
US07039791	05/02/2006	Instruction cache associative crossbar switch
US06892293	05/10/2005	VLIW processor and method therefor
US06185668	02/06/2001	Method and apparatus for speculative execution of instructions
US06360313	09/08/2000	Instruction cache associative crossbar switch
US06047368	04/04/2000	Processor architecture including grouping circuit
US05924125	07/13/1999	Method and apparatus for parallel access to consecutive TLB entries
US05903769	05/11/1999	Conditional vector processing
US05881258	03/09/1999	Hardware compatibility circuit for a new processor architecture
US05560028	09/24/1996	Software scheduled superscalar computer architecture

My VLIW patents US05560028 and US06360313 have so far gained Intergraph Corporation $268 M from Intel and Texas Instruments.

Patent Applications:

- Improved Hybrid Drive
- Method and Apparatus for Reducing Read Latency in a Pseudo Nor Device
- A Memory Having Improved Read Capability
- A Switch for a Two Way Connection Between a Removable Card, a Mobile Wireless Communication Device, or a Computer
- Dynamic Buffer Management In a NAND Memory Controller to Minimize Age Related Performance Degradation Due to Error Correction
- A Method of Operating a NAND Memory Controller to Minimize Read latency Time
- A Method of Storing Blocks of Data in a Plurality of Memory Devices in a Redundant manner, A Memory Controller and a Memory System
- A Method of Storing Blocks of Data in a Plurality of Memory Devices in a Plurality of Memory Devices for High Speed Sequential Read, A Memory Controller and a Memory System

Served as General Chair of Hot Chips Conference in 2003, and Vice Chair in 2002.

PUBLISHED PAPERS:

Siamak Arya, "Using a Managed Memory Subsystem," Electronic Products, September 2007

Siamak Arya, "A Swiss Army Knife for the Memory World," Electronics Weekly, September 2007

Siamak Arya, "Designing High Speed DSPs," Global Signal Processing Conference, 2003

Siamak Arya and Stevan Vlaovic, "System-Level Computer Architecture Simulation: An Experiment Report, " IEEE Int. Performance, Computing, and Communications Conference, 1997

Siamak Arya, Howard Sachs, Sreeram Duvvuru, "An Architecture for High Instruction Level parallelism," 28th Annual Hawaii International Conference on system Sciences, 1995

Sreeram Duvvuru and Siamak Arya, "Evaluation of a Branch Target Address Cache," 28th Annual Hawaii International Conference on system Sciences, 1995

Siamak Arya, "An Integer programming Model for Optimal Register Assignment to Achieve Optimal Instruction Schedules for Super-Computers," Second International Conference on Supercomputing, 1987

Siamak Arya,” An optimal Instruction Scheduling Model for a class of Vector Processors,” IEEE Transactions on Computers, November, 1985

Siamak Arya, “Defining Various Classes of Simulators and Simulations,” Eastern Simulation Conf., 1985

Siamak Arya and D.A. Calahan,”Optimal Scheduling of Assembly Language Kernels for Vector Processors,” Proceedings of Allerton conference, 1982

Short Courses: Attended many project-management, marketing, and software courses, workshops, and seminars